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Search History

DATE: Tuesday, January 03, 2006 Printable Copy Create Case

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DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L23	L20 same l1	3	L23
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L14	L10 same l1	1	L14
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L6	physical adj1 address	14140	L6
L5	L4 same address	37	L5
L4	L3 same l1	44	L4
L3	redundant adj1 word	1087	L3
L2	redundant near2 word	1632	L2
L1	faulty adj1 word	108	L1

END OF SEARCH HISTORY

L5: Entry 13 of 37 File: USPT Sep 21, 1999

DOCUMENT-IDENTIFIER: US 5956350 A
TITLE: Built in self repair for DRAMs using on-chip temperature sensing and heating

Detailed Description Text (13):
Referring now to FIG. 2, a block diagram of one embodiment of the memory array 101 is shown. The memory array 101 includes a ground plane 202, a data write/sense amplifier 204, an address decoder 206, and a plurality of memory cells 208-1 through 208-M. The ground plane 202 is a conductive path held at a constant voltage to shield the signal lines within the memory array from electrical noise. The data write/sense amplifier 204 senses data stored in a row of memory cells during a read operation and drives the detected data on data lines D.sub.0 through D.sub.M-1. The data write/sense amplifier 204 retrieves data from data lines D.sub.0 through D.sub.M-1 and stores the data in a row of memory cells during a write operation. The type of operation being performed by the data write/sense amplifier is controlled by the read/write line. Each row of memory cells is referred to as a word. The row of memory cells being read from or written to is determined by the address decoder 206 which receives an address on lines A.sub.0 through A.sub.r-1 and responsively asserts a word line. The row of cells coupled to the asserted word line can then be accessed for read or write operations. The memory array 101 includes a set of redundant words which can be used in place of faulty words. When a faulty word is detected, subsequent accesses to the address of the faulty word can be redirected to one of the redundant words.

L13: Entry 2 of 5 File: USPT Aug 26, 2003

DOCUMENT-IDENTIFIER: US 6611445 B2
TITLE: Content addressable memory having redundant circuit

Brief Summary Text (22):
In the CAM 62, which uses the conventional redundant-circuit technique, however, since logical addresses (addresses externally input) and physical addresses (addresses actually used at the inside) are mutually converted by the use of the magnitude comparison circuits, the adder, and the subtracter, its circuit has a large scale and a complicated structure. In addition, the circuit 68 for disabling the match output of a defective CAM word is required. The CAM 62 has a large demerit of an increase in area due to the addition of a redundant circuit.

L5: Entry 14 of 37 File: USPT Jun 1, 1999

DOCUMENT-IDENTIFIER: US 5909404 A
TITLE: Refresh sampling built-in self test and repair circuit

Detailed Description Text (14):
Referring now to FIG. 2, a block diagram of one embodiment of the dynamic memory array 101 is shown. The dynamic memory array 101 includes a ground plane 202, a data write/sense amplifier 204, an address decoder 206, a plurality of dynamic memory cells 208-1 through 208-M, and a plurality of weak write circuits 210-1 through 210-M (collectively referred to a weak write circuits 210). The ground plane 202 is a conductive path held at a constant voltage to shield the signal lines within the dynamic memory array from electrical noise. The data write/sense amplifier 204 senses data stored in a row of dynamic memory cells during a read operation and drives the detected data on data lines D.sub.0 through D.sub.M-1. The data write/sense amplifier 204 retrieves data from data lines D.sub.0 through D.sub.M-1 and stores the data in a row of dynamic memory cells during a write operation. The type of operation being performed by the data write/sense amplifier is controlled by the read/write line. Each row of dynamic memory cells is referred to as a word. The row of dynamic memory cells being read from or written to is determined by the address decoder 206 which receives an address on lines A.sub.0 through A.sub.r-1 and responsively asserts a word line. The row of cells coupled to the asserted word line can then be accessed for read or write operations. The dynamic memory array 101 includes a set of redundant words which can be used in place of faulty words. When a faulty word is detected, subsequent accesses to the address of the faulty word can be redirected to one of the redundant words.

L15: Entry 6 of 11 File: USPT Apr 27, 2004

DOCUMENT-IDENTIFIER: US 6728123 B2
TITLE: Redundant array architecture for word replacement in CAM

Brief Summary Text (11):
In one aspect, the invention encompasses a content-addressable memory system with a separate array for word redundancy comprising: a default CAM memory array for storing data; a redundancy latch; a redundant CAM memory array containing redundant word-lines; a redundancy register array for storing at least one respective address of a defective word and for performing the index translation between the redundant array and default memory arrays; a compare logic, coupled to the redundancy memory array.

Detailed Description Text (8):
The redundant array 21, redundant register array (RRA) 22 and compare blocks 23 are shown in FIG. 2. The redundant array 21 provides a number of redundant word lines to be used to replace defective word lines in the default array. The embodiment depicted shows 64 redundant word lines, however this number is arbitrary and up to the discretion of the designer. The RRA 22 portion of the architecture serves a dual purpose: during read/write operations, it acts as a CAM in its own right and tells whether the requested address is mapped to the redundant array and, if so, to which redundant entry. During search operations it acts as a lookup table and converts the m-bit redundant hit index to an n-bit result.

CLAIMS:

1. A content-addressable memory system with a separate array for word redundancy comprising: a default CAM memory array for storing data; a redundancy latch; a redundant CAM memory array containing redundant word-lines; a redundancy register array for storing at least one respective address of a defective word and for performing the index translation between the redundant array and default memory arrays; a compare logic, coupled to the redundancy memory array.

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L15: Entry 11 of 11 File: DWPI Oct 16, 2003

DERWENT-ACC-NO: 2003-864299
DERWENT-WEEK: 200429

TITLE: Semiconductor content-addressable memory system has redundant register array which stores respective address of defective word and performs index translation between redundant array and default arrays

Basic Abstract Text (1):
NOVELTY - A redundant content addressable memory (CAM) array, contains redundant word-lines. A redundant register array (22) stores respective address of a defective word and performs index translation between the redundant CAM array and default CAM arrays (21). A compare logic coupled to the redundant CAM array, produces an index and drive functions for each selected word lines.

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L15: Entry 4 of 11 File: USPT Sep 14, 2004

DOCUMENT-IDENTIFIER: US 6791855 B2
TITLE: Redundant array architecture for word replacement in CAM

Brief Summary Text (11):
In one aspect, the invention encompasses a content-addressable memory system with a separate array for word redundancy comprising: a default CAM memory array for storing data; a redundancy latch; a redundant CAM memory array containing redundant word-lines; a redundancy register array for storing at least one respective address of a defective word and for performing the index translation between the redundant array and default memory arrays; a compare logic, coupled to the redundancy memory array.

Detailed Description Text (8):
The redundant array 21, redundant register array (RRA) 22 and compare blocks 23 are shown in FIG. 2. The redundant array 21 provides a number of redundant word lines to be used to replace defective word lines in the default array. The embodiment depicted shows 64 redundant word lines, however this number is arbitrary and up to the discretion of the designer. The RRA 22 portion of the architecture serves a dual purpose: during read/write operations, it acts as a CAM in its own right and tells whether the requested address is mapped to the redundant array and, if so, to which redundant entry. During search operations it acts as a lookup table and converts the m-bit redundant hit index to an n-bit result.

L15: Entry 3 of 11 File: USPT Jan 4, 2005

DOCUMENT-IDENTIFIER: US 6839257 B2
TITLE: Content addressable memory device capable of reducing memory capacity

Brief Summary Text (17):
As the memory capacity of CAM increases and the sizes of device elements decrease, improvement in production yield becomes more important. In addition to controlling the production process, it is known to improve in the production yield by designing CAM devices taking into account the possibility that CAM devices may include a certain number of failed words. For example, a certain number of redundant (spare) words are prepared in each bank so that a failed word can be replaced with a redundant word.

Brief Summary Text (18):
However, when the memory capacity of the CAM device increases, the memory capacity of each bank increases and thus the number of failed words in each bank also increases. When a bank includes a large number of failed words, all failed words cannot be replaced with redundant words prepared in that bank, and consequently that CAM device cannot be used.

Detailed Description Text (54):
The bit indicating the bank number of a bank 20, the bit indicating an address of a word in the bank 20, the bit indicating a plane, and a dummy bit used in the address conversion are not limited to specific bits. Those bits may be assigned to arbitrary bits in an address. Furthermore, in the CAM according to the present invention, a redundant word may be provided in a bank or a plane such that it can be used instead of a failed word thereby avoiding the bank or plane from becoming unusable. This allows a further improvement in production yield of CAM devices.

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L15: Entry 1 of 11 File: USPT Jul 19, 2005

DOCUMENT-IDENTIFIER: US 6920525 B2
TITLE: Method and apparatus of local word-line redundancy in CAM

CLAIMS:

6. A method of redundancy of word-lines in a content-addressable memory (CAM) having the ability to store the redundancy repair data pattern in redundant word-lines in said CAM, comprising the step of testing read/write operation on word-lines by using a BIST (built-in self-test) and storing failing word-line address locations, wherein word-lines and match-lines are steered so that match-lines remain coincident with word-lines.

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L22: Entry 1 of 1 File: USPT Oct 16, 2001

DOCUMENT-IDENTIFIER: US 6304498 B1
TITLE: Semiconductor memory device capable of suppressing degradation in operation speed after replacement with redundant memory cell

Detailed Description Text (17):
Normal row decoder 140.i selects a memory cell row (word line WL) of a corresponding normal memory cell block MCBi based on a row predecode signal transmitted by a row predecode line group PDL. Redundant row decoder 142.i selects a redundant memory cell row (redundant word line SWL) of a corresponding redundant memory cell block RCBi based on an instruction from a corresponding spare determination circuit 40.i and on a predecode signal from row predecoder 26. When the selection of the redundant memory cell row is performed by redundant row decoder 142.i, the row select operation by normal row decoder 140.i is stopped.

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US 20050071723A1

(19) United States

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Luick (43) Pub. Date: Mar. 31, 2005

(54) ADAPTIVE RUNTIME REPAIRABLE ENTRY REGISTER FILE

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(52) U.S. Cl. 714/747

(57) ABSTRACT

Methods and apparatus are disclosed that provide for improved addressing of a register file in a computer system. The register file has one or more redundant words. A logical address in an instruction is mapped, during a predecode operation, to a physical address having a larger address space than the logical address. Addresses of nonfaulty words are mapped to the same word in the larger address space as the logical address. Logical addresses that point to faulty words are mapped to a redundant word that is in the larger address space but not in the address space of the logical address. Because all addresses presented to a register file decoder at access time point to nonfaulty words, no delay penalty associated with address compare during the access time is required.